An RF CMOS Transmitter Integrating a Power Amplifier and a Transmit/Receive Switch for 802.11b Wireless Local Area Network Applications

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Abstract — **A transmitter integrating a passive FET Quad up-conversion mixer, a power amplifier with output P_{1dB} of 23 dBm, a transmit/receive (T/R) switch with an insertion loss of 1.1 dB and output P_{1dB} of 21 dBm has been implemented in a 0.25-μm foundry CMOS process. The transmitter at the output power level of 16.5 dBm is compliant to the 802.11b specifications at 11 Mbps. This circuit is the first 802.11b transmitter to have the entire function integrated including a PA and a T/R switch.**

I. Introduction

Wireless Local Area Network (WLAN) applications have emerged as the fastest growing opportunity for the RF integrated circuits industry. With the growth of this market, the bill of material for a radio has been rapidly eroding, therefore, cost reduction has become the key to success. To address this, a transmitter for 802.11b WLAN applications, which integrates a passive FET Quad up-conversion mixer, driver, power amplifier with output P_{1dB} of 23 dBm, transmit/receive (T/R) switch with an insertion loss of 1.1 dB and output P_{1dB} of 21 dBm, voltage doubler, and control logic circuit for the T/R switch has been implemented in a 0.25-μm foundry CMOS process. The transmitter at the output power level of 16.5 dBm is compliant to the 802.11b side-lobe specifications at 11 Mbps.

II. Circuits Design

The transmitter is shown in Fig. 1. It takes signals from the Baseband Processor (BBP) and up-converts them directly to the 2.4 GHz ISM band using dual passive FET quad mixers. The FET quad mixers were chosen for their high linearity since the BBP digital to analog converter (DAC) outputs could be on the order of 1 Vp-p differential, which could easily saturate typical current mode mixers operating with a 3 V supply. The mixer outputs are connected together, in quadrature modulator

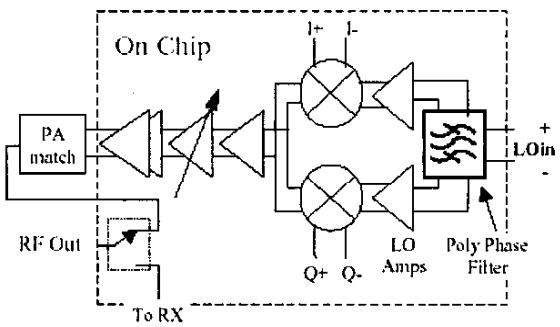

Figure 1: Transmitter w/ T/R switch block diagram

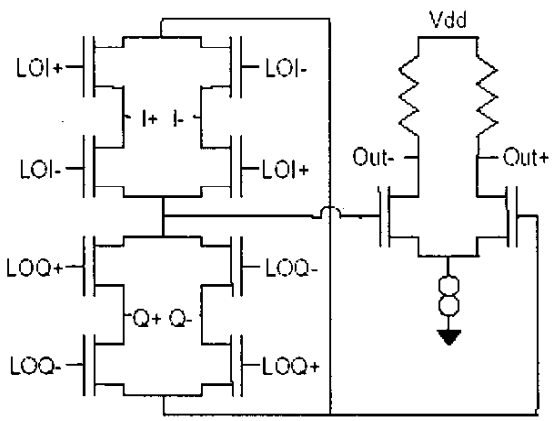

Fig. 2: Simplified mixer and sum amp schematic

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fashion [1], at the input of a differential summing amplifier with resistive loads. Fig. 2 shows a simplified schematic of the quadrature mixers and summing amplifier. LO signal is supplied from off-chip with quadrature signals created via an on-chip 2-pole polyphase filter. A final LO amplifier boosts drive levels up to rail-to-rail and turns LO signal into a square wave for maximum mixer gain. The output of the summing amplifier provides the input to the power amplifier stages.

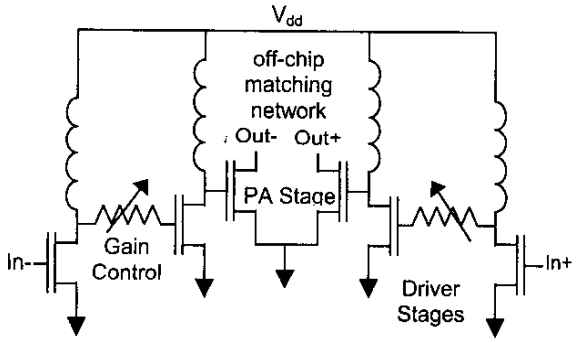

Figure 3: Simplified power amplifier schematic

Fig. 3 shows a simplified schematic of the driver and power amplifier. There are 3 stages with a variable attenuator in between the 1st and 2nd stages. The first two stages form the driver, which consists of inductively loaded pairs of transistors differentially driven with 10 and 12 dB of gain respectively. The power amplifier, or the third stage, is also a pair of differentially driven transistors with drain biasing, matching, and balun functions performed off chip. The power amplifier has 7.5 dB of gain. P_{1dB} of the amplifier is 23 dBm with a power added efficiency (PAE) of 29%, at output P1dB, and OIP3 of 32.1dBm.

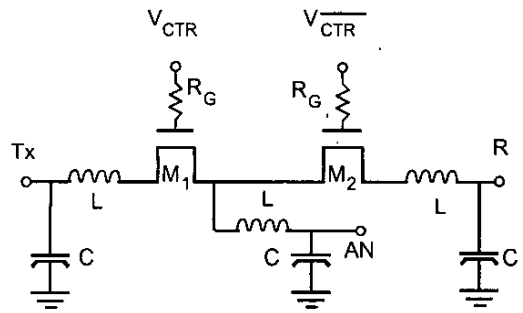

Fig. 4(a): T/R switch schematic

Fig. 4(a) shows the switch schematic. The switch core contains two transistors [2], one for the transmitter chain and the other for the receiver. The two transistors are identical. In order to improve power handling capability, drain and source nodes are biased to 3 V and the RF voltage seen by the transistors is reduced by transforming the impedances seen by the transistors down to ~25 Ω [3],[4],[5]. The transformation is accomplished using a series L-shunt C matching network. The series L is formed using bondwire and package parasitic inductance, and the shunt C is realized with an off-chip capacitor. When the impedances seen by the switch transistors are reduced, the transistor on-resistance to load impedance ratio increases. This increases switch insertion loss, and the switch design must balance insertion loss and P_{1dB} to provide adequate performance at the desired maximum output power level.

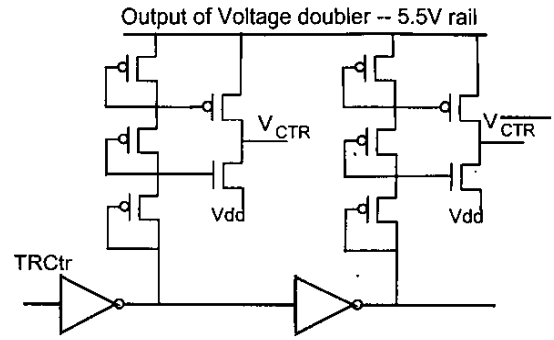

Fig. 4(b): logic control circuit schematic

Biasing the drains and sources of the switch transistors to 3 V to increase P_{1dB} and lower insertion loss [5] requires switch control voltage (V_{CTRL}) greater than 5 V. A voltage doubler and switch control logic circuit operating at 5.5 V are integrated on the same chip to enable operation using a single 3 V supply. The voltage doubler is a charge pump cell type with improved PMOS serial switches [6]. The 22 MHz reference clock signal for the radio is used to provide input signals for the voltage doubler. The control logic circuit is shown in Fig. 4(b). To satisfy the reliability requirement, the circuit is implemented using 3.3 V I/O transistors, and gate-to-drain and drain-to-source voltages in the logic circuit are kept less than 2.5 V despite the fact that the output of the circuit swings between 3.0 and 5.5 V.

III. Experiment Results

The measured unwanted sideband rejection and carrier suppression for the transmitter were both approximately 40 dB relative to the upper sideband, which indicates a quadrature error of approximately 1 degree, amplitude error of approximately 0.1dB, and low DC offsets. Insertion loss and isolation of the switch versus frequency

2.4GHz input power(dBm)	2.4GHz output power(dBm)	4.8 GHz 2nd harmonic(dBm/MHz)	7.2 GHz 3rd harmonic(dBm/MHz)
20	18.88	-49.5	-51.5
21	19.47	-46.5	-47.4
22	20.2	-44.8	-44.8

Table 1: Switch harmonic response at 11 Mbps QPSK input signal

are shown in Fig. 5. The measured insertion loss for the switch is 1.1 to 1.2 dB and isolation is 19.5 to 20.2 dB at frequencies between 2.4 and 2.5 GHz. The low insertion loss and reasonable isolation are realized by lowering substrate resistances [5]. Output power versus input power plot for the switch is shown in Fig. 6. P_{1dB} compression point of the switch is 21 dBm at 2.4 GHz.

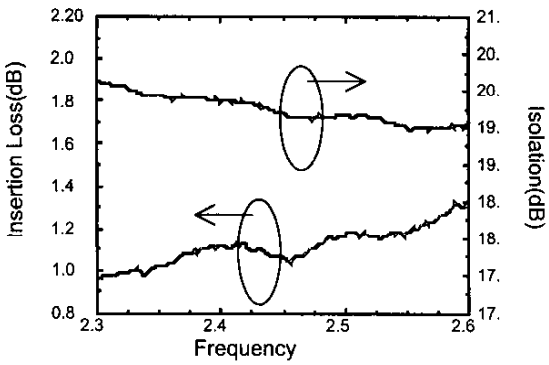

Figure 5: Measured switch insertion loss and isolation

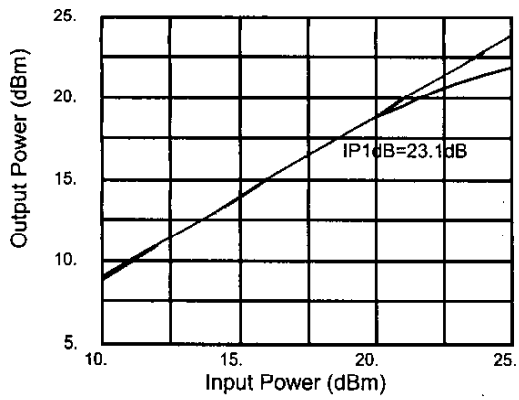

Figure 6: Measured switch 1dB compression point

The FCC requires that power emissions at the 2nd and 3rd harmonic frequencies be less than -41.25 dBm/MHz. In the case of the T/R switch, the output is bandpass filtered and the high order harmonics are suppressed. The same T/R switch can also be used as an antenna diversity switch, however, there is no succeeding filter so harmonic response of the switch is critical. To ensure compliance harmonic response of the switch was characterized by applying a QPSK signal with an 11 Msps data rate. Table 1 shows that even at an input power of 22 dBm, the output power levels of the 2nd and 3rd harmonics are less than -44 dBm/MHz even without any filtering effects. In addition, when the diversity switch and power amplifier are integrated on the same chip, the signal from the PA can directly couple to the output of the diversity switch through the common substrate and bypass the channel filter. In order to characterize this coupling, the switch output power has also been measured when the connection between the PA and the switch is broken. At the PA output power of 18.0 dBm, the 2nd and 3rd harmonic powers are less than –55dBm/MHz. These results indicate that a diversity switch can also be integrated with the transmitter without violating the FCC regulations.

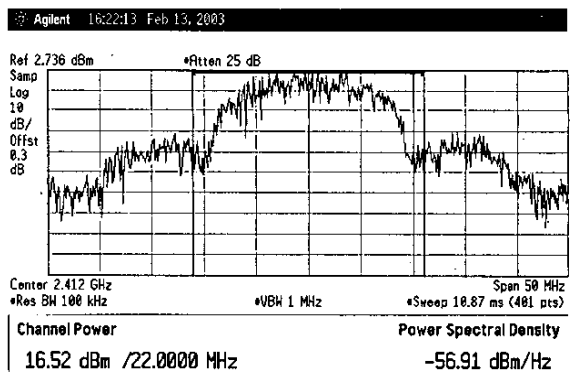

Figure 7: Integrated Output Power

Integrated output power, shown in Fig. 7, is 16.5 dBm for the entire transmitter chain, including the switch, under the modulation of an 11 Msps QPSK signal and V_{DD} of 3 V. At this power level the output spectrum satisfies the side-lobe requirements for 802.11b as shown in Fig. 8, with the dark line representing the specification. The output P_{1dB} compression point for the entire transmitter is 17.5 dBm. The compression of the

transmitter chain is currently limited by the up-conversion mixer. The current consumption of the chain is 335 mA.

The PA and switch combination was stressed at the PA output power level of +23.0 dBm and at room temperature, for more than 3 months. No apparent shifts in the PA and switch characteristics were observed. The switch and PA have also been stressed by mismatching the output to a 20:1 VSWR. The switch, PA, as well as PA/switch combination survived the stress at 20 dBm output power. Fig. 9 shows the die photograph of the transmitter chain. The active area is <4.5 mm^2. The transmitter was tested in a LPCC package.

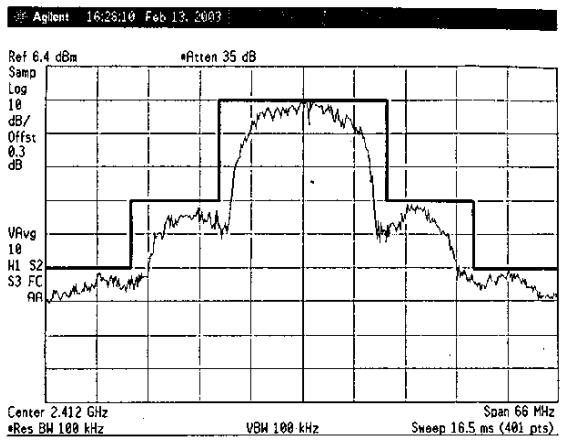

Figure 8: Output Mask with Specification

TX & Switch P1dB	**17.5 dBm**
PA/Driver current	**284 mA**
Modulator current	**8.6 mA**
LO Buffer (I & Q) current	**42 mA**
Voltage Doubler current	**640 µA**
Supply Voltage	**3.0 V**
Technology	**0.25 µm 1P5M CMOS**
Die Area	**<4.5 mm^2**
Package	**LPCC**

Table 2: Performance Summary

IV. Conclusion

A transmitter with integrated PA and T/R switch is demonstrated. The transmitter output spectrum meets the 802.11b side-lobe specifications at 11 Mbps with 16.5 dBm output power. This is the first transmitter for 802.11b applications to have the entire function integrated including a PA and a T/R switch. The transmitter can be integrated with a receiver to implement a single chip transceiver. Typical performance is summarized in Table 2.

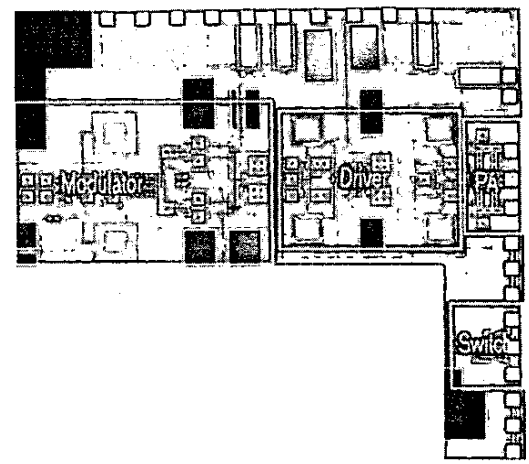

Fig. 9: Microphotograph of die.

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